IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Chung K. Chin
Case:	Terablaze 4
Serial No.:	10/552,601
Filing Date:	October 5, 2005
Group:	2476
Examiner:	Chuong T. Ho
Title:	Method and Apparatus for Shared Multi-Bank Memory

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby appeals the non-final rejection dated September 29, 2010 of claims 1-8 and 18-24 of the above-identified patent application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc., as evidenced by the statement under 37 CFR 3.73 (b) submitted on January 4, 2007. The assignee, Agere Systems Inc., is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on October 5, 2005 with claims 1 through 24. Claims 14-17 were cancelled in the Amendment and Response to Office Action dated October 7,

2008. Claims 1-13 and 18-24 are presently pending in the above-identified patent application. Claims 1, 4, 7, 8, 18, 21, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. (United States Patent No. 6,021,132) in view of Sindhu et al. (United States Patent No. 7,116,660), claims 2 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al., and further in view of Benson et al. (United States Patent No. 6,151,321), claims 3 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al., and further in view of Kamaraj et al. (United States Patent No. 6,501,757), claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al., and further in view of Beshai (United States Publication No. 2004/0184448), claims 6 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. and Sindhu et al., in view of Lavelle et al. (United States Patent No. 6,812,929), and claim 24 is rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. and Sindhu et al., in view of Manning et al. (United States Patent No. 6,088,736). The Examiner indicated that claims 9-13 are allowed.

Claims 1, 2, 6, 18, 19, and 22 are being appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the non-final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a method for storing a packet in a shared memory in a packet switch, the method comprising the step of:

storing in the shared memory (FIG. 1: 114), wherein the shared memory comprises two or more buffers (FIG. 1: 118; page 4, lines 29-30) and two or more banks (FIG. 1: 116), at least a portion of a packet in contiguous banks of a first buffer of the two or more buffers (page 9, lines 13-15), wherein each of the banks comprises portions (FIG. 1), wherein each of the two or more buffers comprises a portion from each of the plurality of banks (FIG. 1), and wherein each of the buffers identifies an address of a location in each of the banks (page 4, lines 30-31).

Claims 2 and 19 require wherein the packet comprises a plurality of portions, and further comprising the step of storing an additional portion of the packet in contiguous banks of a

second buffer if one of the portions is stored in a last bank of the first buffer and the portion stored in the last bank of the first buffer is not a last portion of the packet (page 9, lines 15-18).

Claims 6 and 22 require wherein the banks are divided into a first set of banks and a second set of banks, and further comprising the step of allocating a buffer that comprises one or more banks from the first set and a buffer that comprises one or more banks from the second set in response to a buffer request (page 38, lines 4-18).

Independent claim 18 is directed to a shared memory (FIG. 1: 114) for storing a packet, comprising:

two or more buffers (FIG. 1: 118; page 4, lines 29-30) and two or more banks (FIG. 1: 116), wherein each of the banks comprises portions (FIG. 1), wherein each of the two or more buffers comprises a portion from each of the plurality of banks (FIG. 1), wherein each of the buffers identifies an address of a location in each of the banks (page 4, lines 30-31), and wherein at least a portion of the packet is stored in contiguous banks of a first buffer of the two or more buffers (page 9, lines 13-15).

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 4, 7, 8, 18, 21, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al., claims 2 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al., and further in view of Benson et al., claims 3 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al., and further in view of Kamaraj et al., claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al., and further in view of Beshai, claims 6 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. and Sindhu et al., in view of Lavelle et al., and claim 24 is rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. and Sindhu et al., in view of Manning et al.

ARGUMENT

Independent Claims 1 and 18

Independent claims 1 and 18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al. Regarding claim 1, the Examiner asserts

that Sindhu discloses storing in said shared memory (FIG. 9, shared memory), wherein said shared memory comprises two or more buffers (FIG. 9: M (0), M (1), M (2), M (3), M (4), M (5), M (6), M (7)), at least a portion of a packet in contiguous banks (FIG. 9, banks 902) of a first buffer (M (0)) of said two or more buffers, wherein each of said banks (FIG. 9, banks 902) comprises portions, wherein each of said two or more buffers comprises a portion from each of said plurality of banks, and wherein each of said buffers identifies an address of a location in each of said banks (col. 14, lines 30-35). In the Advisory Action dated December 14, 2009, the Examiner asserts that Muller discloses where each of said two or more buffers comprises a portion from each of said plurality of banks (col. 8, lines 43-45; the buffers may be further subdivided into a number of memory lines).

Appellants note that Sindhu teaches that FIG. 9 illustrates a *reservation table 508* that "includes a *plurality of columns* 900, *one for each memory bank 105 in global data buffer 104,* a *plurality of rows* 902" (col. 11, lines 22-26; emphasis added) and that "*each row represents a set of read requests*" (col. 11, lines 26-27; emphasis added). Thus, contrary to the Examiner's assertion, FIG. 9 does *not* represent a shared memory (as defined in the context of the present invention and as is well known in the art); the columns of table 508 are *not* buffers; and the rows of table 508 are *not* banks. Furthermore, Sindhu's teaching at col. 14, lines 30-35, refers to memory banks 105 of FIG. 2B (see, cols. 12-14); Sindhu's teaching at col. 14, lines 30-35, does *not* refer to the rows 902 of table 508.

Furthermore, as the Examiner previously acknowledged, Muller teaches that the buffers may be further *subdivided into a number of memory lines*; Muller does *not* disclose or suggest where each of the buffers *comprise a portion from* ***each*** *of said plurality of banks*.

In the Response to Arguments section of the present Office Action, the Examiner equates the claimed two or more buffers with buffers #1-3 (FIG. 3A) of Muller. The Examiner also equates the claimed banks with buffers #1-3 (FIG. 3A) of Muller and equates the claimed first buffer with the shared memory 230 of FIG. 3A. Appellants find no logic in the apparent inconsistency of equating the claimed buffers and banks with the same entities in Muller. It is noted that the cited claims require wherein each of said banks comprises portions, and wherein each of said two or more buffers comprises a portion from each of said plurality of banks.

Furthermore, neither Muller nor Sindhu, alone or in combination, disclose or suggest that a *shared memory comprises two or more buffers and two or more banks, wherein*

each of the banks comprises portions, *wherein* ***each of the two or more buffers comprises a portion from each of the plurality of banks***, *and wherein each of the buffers identifies an address of a location in each of the banks*.

Thus, Muller et al. and Sindhu et al., alone or in combination, do not disclose or suggest wherein said shared memory comprises two or more buffers and two or more banks, at least a portion of a packet in contiguous banks of a first buffer of said two or more buffers, wherein each of said banks comprises portions, wherein each of said two or more buffers comprises a portion from each of said plurality of banks, and wherein each of said buffers identifies an address of a location in each of said banks, as required by independent claims 1 and 18.

Claims 2 and 19

Claims 2 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. in view of Sindhu et al., and further in view of Benson et al. In particular, the Examiner acknowledges that Muller and Sindhu do not explicitly teach said data unit stored in said last bank of said first buffer is not a last data unit of said packet, but asserts that Benson teaches storing an additional portion (the rest of the cell of the packet) of said packet in a second buffer (the second card buffer) if one of said portions (the cell of the packet) is stored in said first buffer (the first card buffer) and said portions stored in said first buffer (the first card buffer) is not a last portion of said packet (FIG. 7B, place enough data in the first card buffer to fill the host buffer, place the rest of the cell into the second card buffer).

As the Examiner notes, FIG. 7B of Benson teaches placing enough data in the first card buffer to fill the host buffer, and placing the rest of the cell into the second card buffer. Benson, however, does *not* disclose or suggest *storing an additional portion of a packet in contiguous banks of a second buffer if one of the portions is stored in a last bank of a first buffer and a portion stored in the last bank of the first buffer is not a last portion of the packet.*

Thus, Muller et al., Sindhu et al., and Benson et al., alone or in combination, do not disclose or suggest wherein said packet comprises a plurality of portions, and further comprising the step of storing an additional portion of said packet in contiguous banks of a second buffer if one of said portions is stored in a last bank of said first buffer and said portion stored in said last bank of said first buffer is not a last portion of said packet, as required by claims 2 and 19.

Claims 6 and 22

Claims 6 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over Muller et al. and Sindhu et al., in view of Lavelle et al. In particular, the Examiner acknowledges that Muller and Sindhu do not explicitly teach, but asserts that Lavelle teaches wherein said banks are divided into a first set of banks and a second set of banks, and a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set (col. 14, lines 59-62; a frame buffer, wherein the frame buffer includes a first set of one or more banks, a second set of one or more memory banks).

Appellant notes that, in the text cited by the Examiner, Lavelle teaches:

> a frame buffer, wherein the frame buffer includes a first set of one or more memory banks, a second set of one or more memory banks, and a cache, wherein the frame buffer is configured to load data from the first set into the cache in response to receiving a cache fill request targeting the first set, wherein the first set is accessible independently of the second set
> (Col. 14, lines 59-62; emphasis added.)

Lavelle teaches a frames buffer that contains two sets of banks; Lavelle does *not* disclose or suggest ***a*** *buffer that comprises one or more banks from a first set of banks* ***and a*** *buffer that comprises one or more banks from a second set of banks.* Lavelle also does *not* disclose or suggest *allocating* a buffer that comprises one or more banks from a first set of banks and a buffer that comprises one or more banks from a second set of banks *in response to a buffer request*.

Thus, Muller et al., Sindhu et al., and Lavelle et al., alone or in combination, do not disclose or suggest wherein said banks are divided into a first set of banks and a second set of banks, and further comprising the step of allocating a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set in response to a buffer request, as required by claims 6 and 22.

Conclusion

The rejections of the cited claims under section 103 in view of Muller et al., Sindhu et al., Benson et al., Kamaraj et al., Beshai, Lavelle et al., and Manning et al., alone or in any combination, are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,

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CLAIMS APPENDIX

1. A method for storing a packet in a shared memory in a packet switch, said method comprising the step of:

storing in said shared memory, wherein said shared memory comprises two or more buffers and two or more banks, at least a portion of a packet in contiguous banks of a first buffer of said two or more buffers, wherein each of said banks comprises portions, wherein each of said two or more buffers comprises a portion from each of said plurality of banks, and wherein each of said buffers identifies an address of a location in each of said banks.

2. The method of claim 1, wherein said packet comprises a plurality of portions, and further comprising the step of storing an additional portion of said packet in contiguous banks of a second buffer if one of said portions is stored in a last bank of said first buffer and said portion stored in said last bank of said first buffer is not a last portion of said packet.

3. The method of claim 1, wherein each of said two or more buffers comprises one or more groups and each of said groups comprises a plurality of banks.

4. The method of claim 1, wherein at least a portion of each of two or more packets are stored in one of said buffers.

5. The method of claim 1, further comprising the step of cyclically accessing one or more data ports, each of said data ports corresponding to one or more of said plurality of banks.

6. The method of claim 1, wherein said banks are divided into a first set of banks and a second set of banks, and further comprising the step of allocating a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set in response to a buffer request.

7. The method of claim 1, wherein said shared memory exchanges packets between ports in said packet switch.

8. The method of claim 1, wherein sequential data units of said packet are stored in contiguous banks of at least one of said two or more buffers.

9. A method for managing a shared memory in a packet switch, said shared memory comprising one or more buffers, said method comprising the step of:

maintaining a buffer usage count for at least one of said buffers, wherein said buffer usage count provides an indication of a sum over all packets in said at least one of said buffers of a number of output ports toward which each of said packets is destined, wherein said at least one of said buffers contains two or more packets and wherein at least one of said two or more packets is destined for more than one output port; and

adding said at least one of said buffers to a free buffer list if a release of said at least one of said buffers does not occur within a predefined period of time.

10. The method of claim 9, further comprising the step of incrementing said buffer usage count by one to indicate that a packet destined for one output port is stored in said buffer.

11. The method of claim 9, further comprising the step of decrementing said buffer usage count by one when a data unit is read from said buffer and said data unit is the last data unit of a packet or the last data unit of said buffer.

12. The method of claim 9, wherein said buffer usage count indicates a number of destination ports for a packet to perform a multicasting operation.

13. The method of claim 9, further comprising the step of determining whether a buffer is free based on said buffer usage count.

14. (Cancelled)

15. (Cancelled)

16. (Cancelled)

17. (Cancelled)

18. A shared memory for storing a packet, comprising:

two or more buffers and two or more banks, wherein each of said banks comprises portions, wherein each of said two or more buffers comprises a portion from each of said plurality of banks, wherein each of said buffers identifies an address of a location in each of said banks, and wherein at least a portion of said packet is stored in contiguous banks of a first buffer of said two or more buffers.

19. The shared memory of claim 18, wherein said packet comprises a plurality of portions, and wherein an additional portion of said packet is stored in contiguous banks of a second buffer if one of said portions is stored in a last bank of said first buffer and said portion stored in said last bank of said first buffer is not a last portion of said packet.

20. The shared memory of claim 18, wherein each of said two or more buffers comprises one or more groups and each of said groups comprises a plurality of banks.

21. The shared memory of claim 18, wherein at least a portion of each of two or more packets are stored in one of said buffers.

22. The shared memory of claim 18, wherein said banks are divided into a first set of banks and a second set of banks, and further comprising the step of allocating a buffer that comprises one or more banks from said first set and a buffer that comprises one or more banks from said second set in response to a buffer request.

23. The shared memory of claim 18, wherein said shared memory exchanges packets between ports in a packet switch.

24. The shared memory of claim 18, further comprising a counter for monitoring a buffer usage count that provides an indication of the sum over all packets in said at least one of said buffers of the number of output ports toward which each of said packets is destined.

EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.